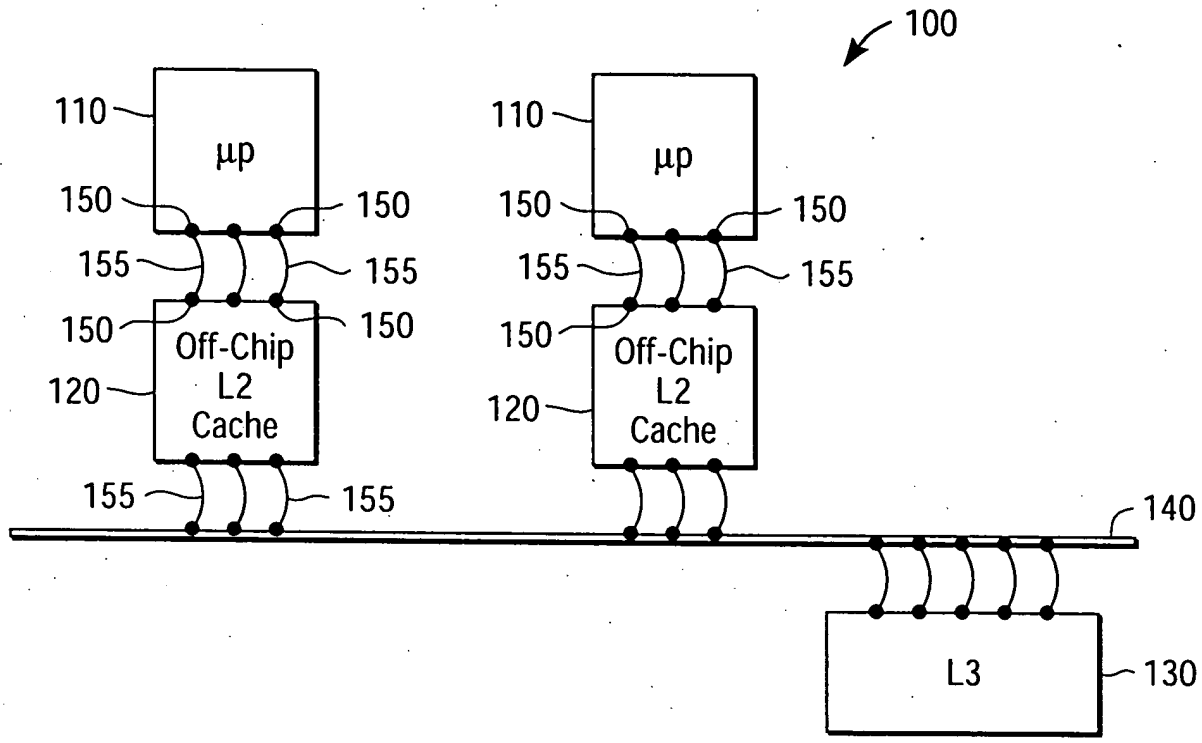

FIG. 1 (PRIOR ART)

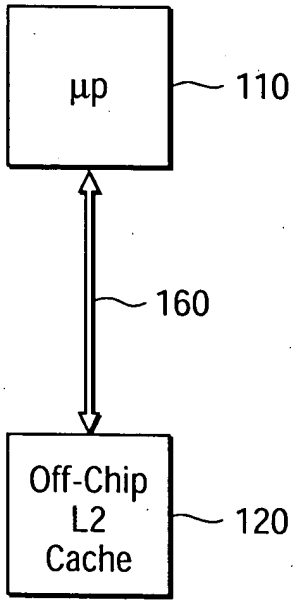

FIG. 2A (PRIOR ART)

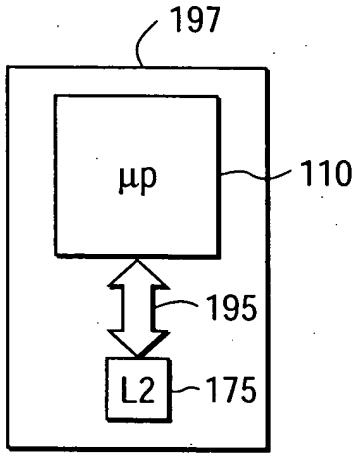

FIG. 2B (PRIOR ART)

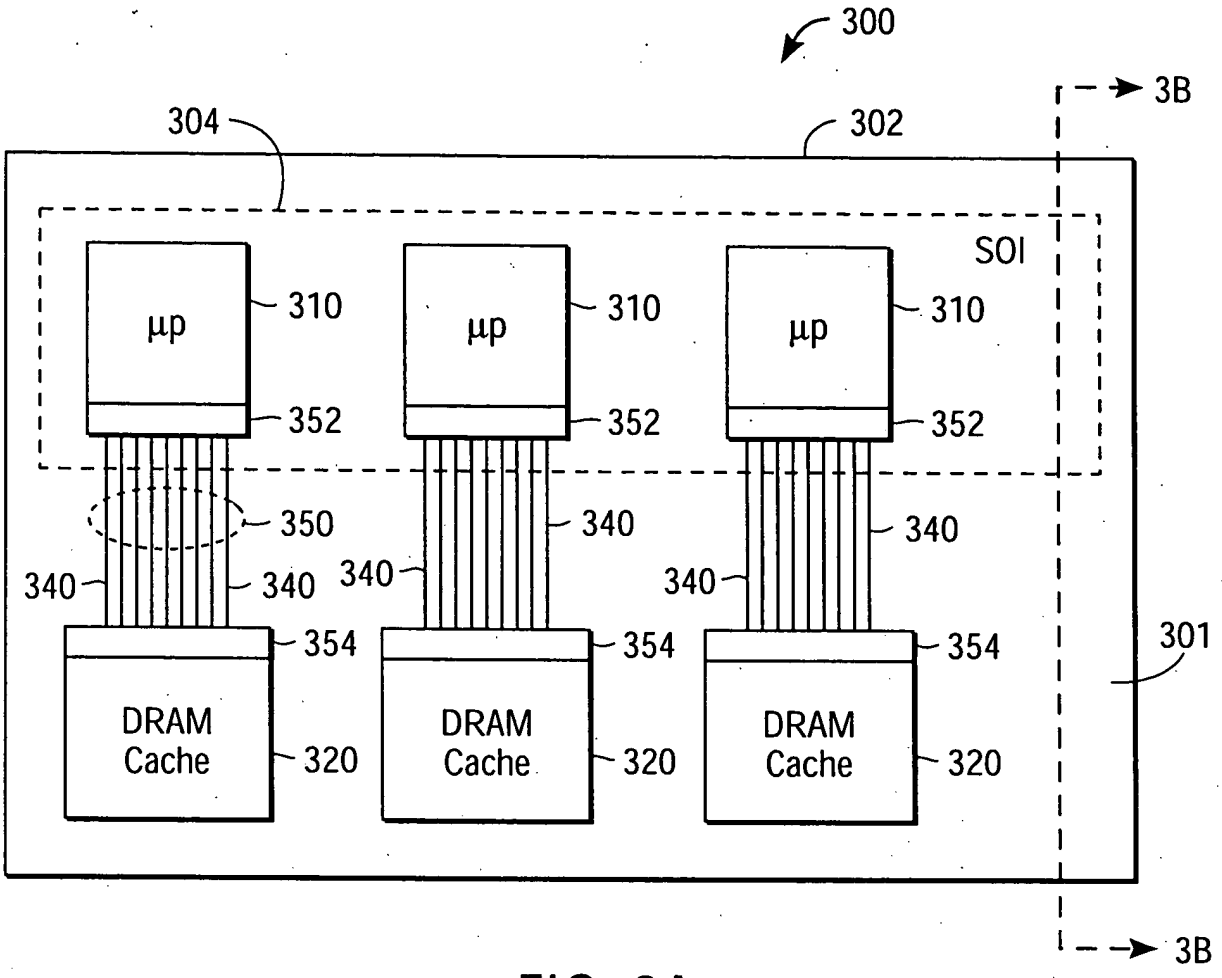
300
3B
304
302
SOI
µp
310
352
350
340
354
DRAM Cache
320
301
3B

FIG. 3A

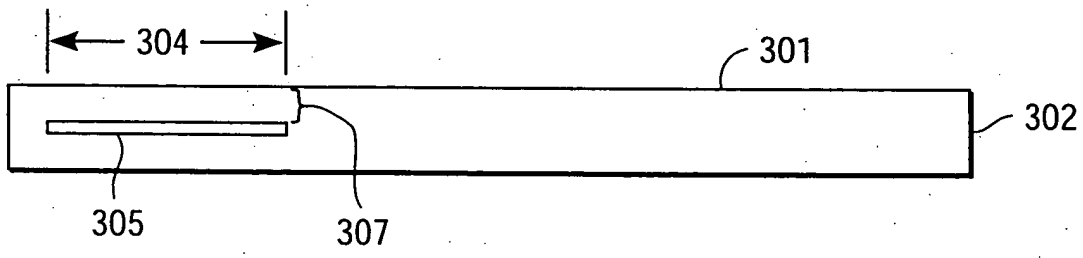
304
301
302
305
307

FIG. 3B

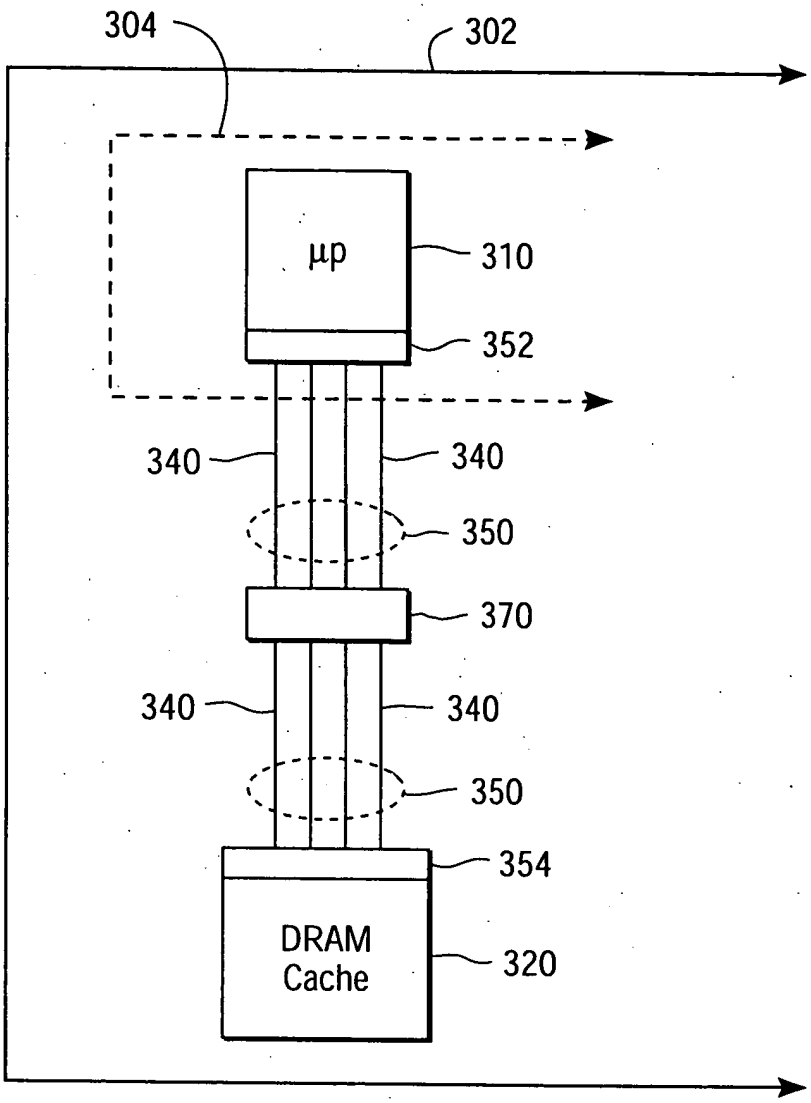
304
302
µp
310
352
340
340
350
370
340
340
350
354
DRAM
Cache
320

FIG. 4

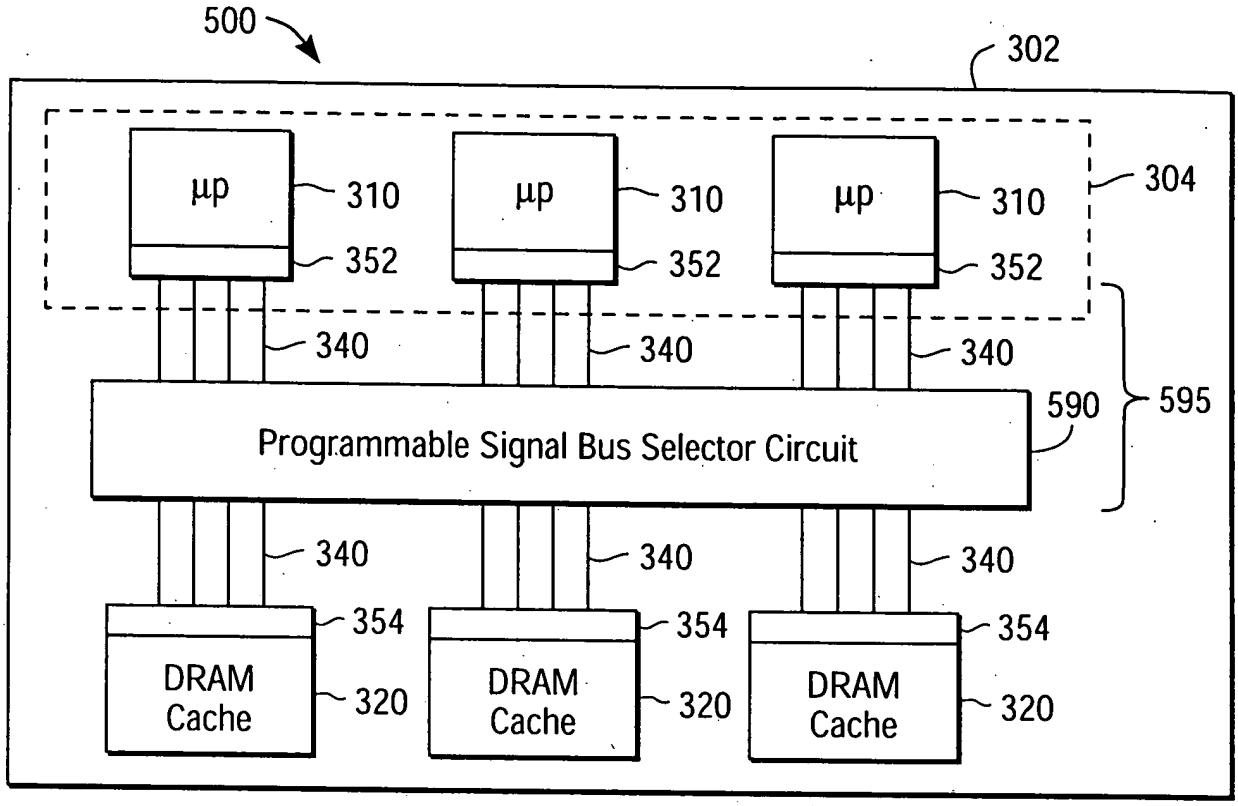
500
302
µp
310
352
304
340
590
595
Programmable Signal Bus Selector Circuit
354
DRAM Cache
320

FIG. 5A

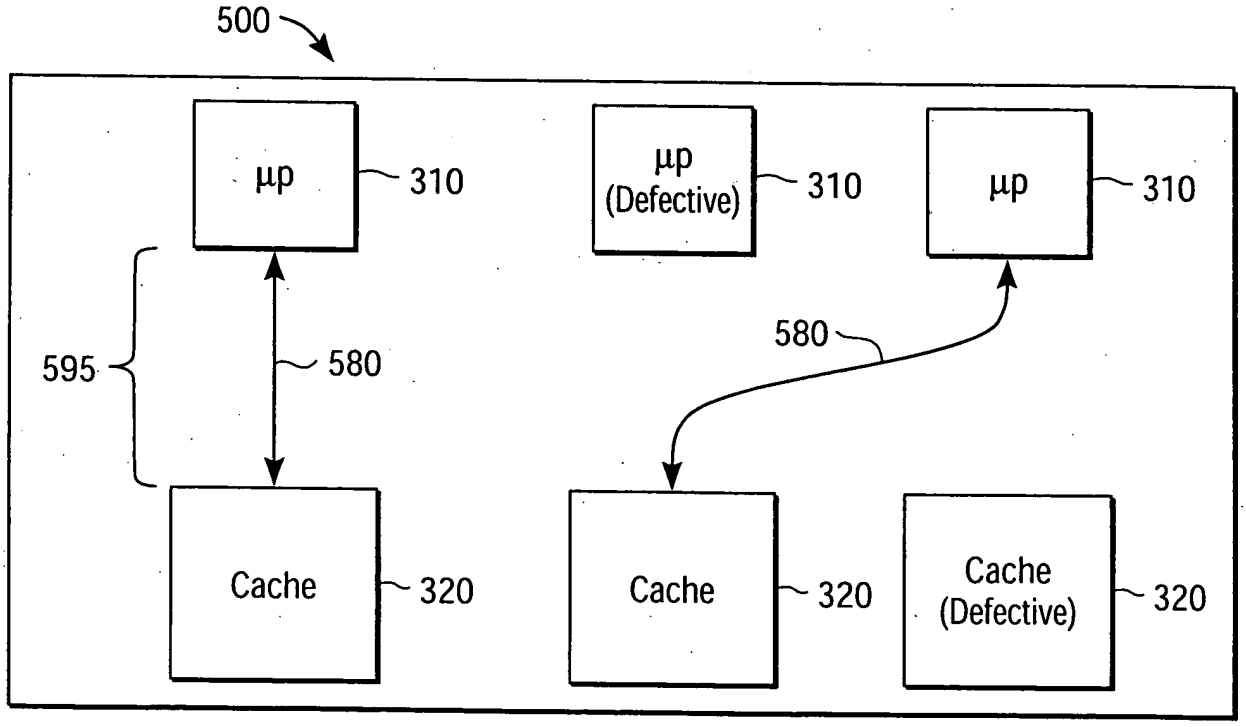
500
µp
310
µp (Defective)
595
580
Cache
320
Cache (Defective)

FIG. 5B

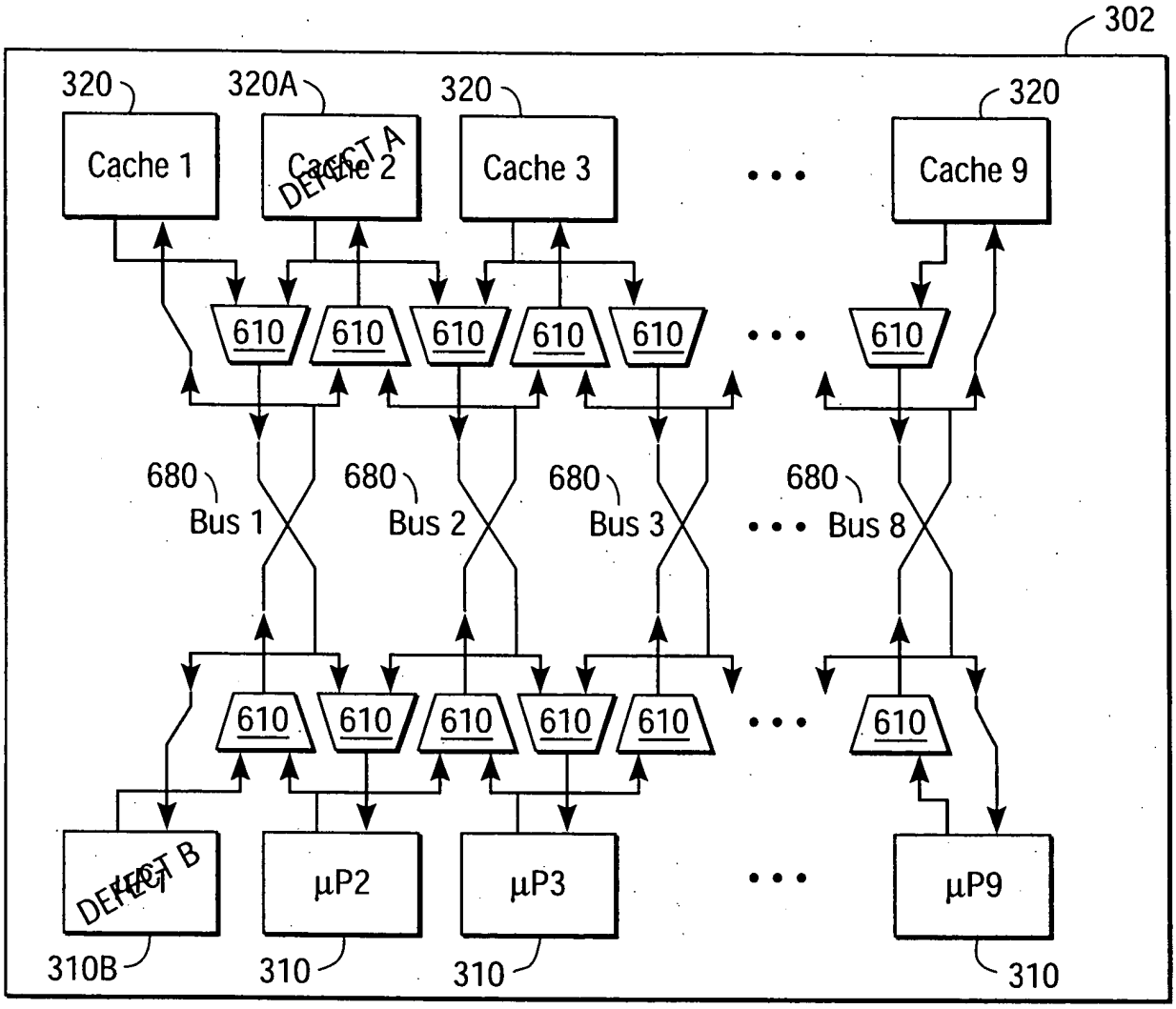
302
320
320A
320
320
Cache 1
DEFECT A
Cache 2
Cache 3
Cache 9
610
680
Bus 1
Bus 2
Bus 3
Bus 8
DEFECT B
µP2
µP3
µP9
310B
310
310
310

FIG. 6

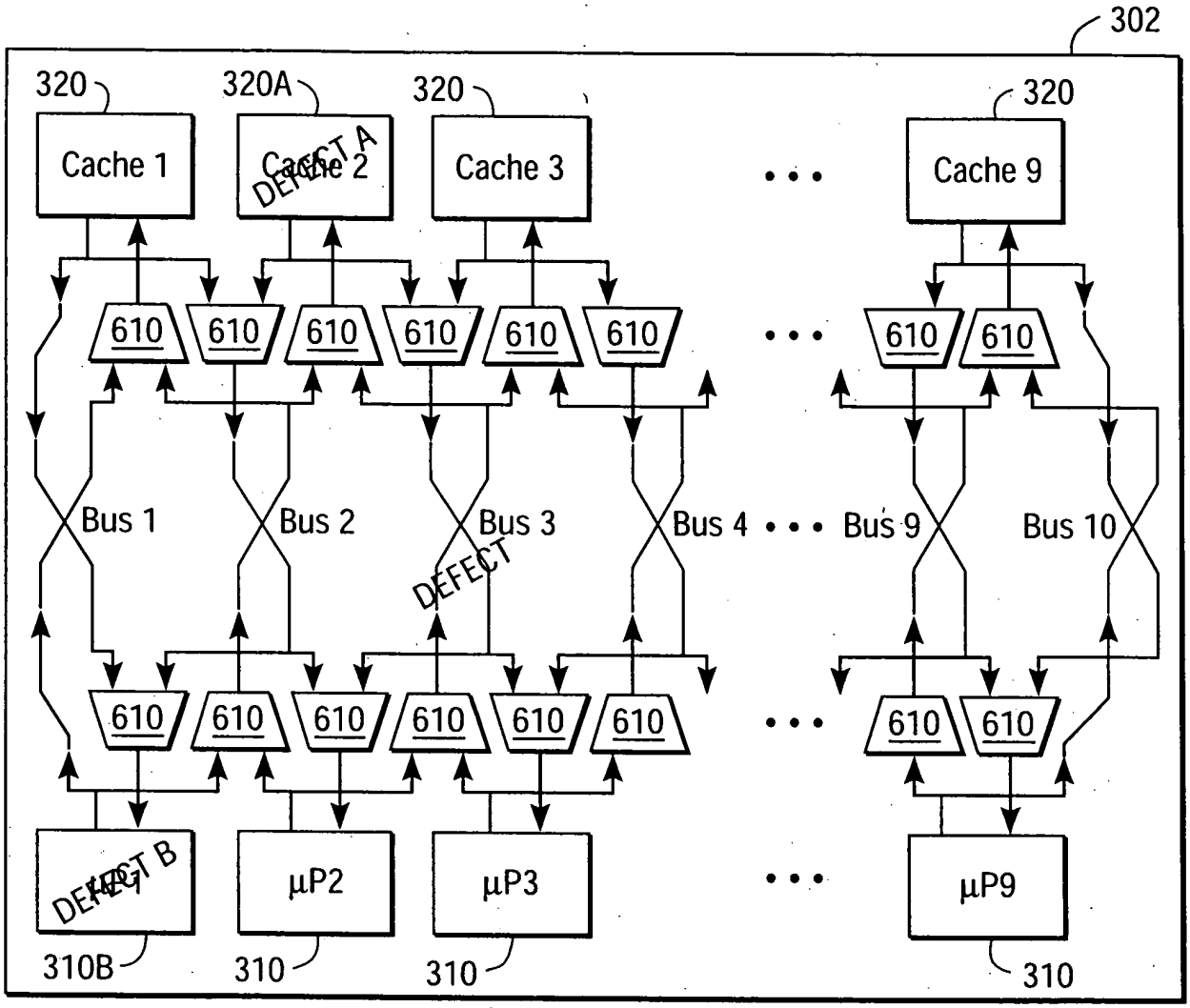
302
320
320A
320
320
Cache 1
Cache 2
DEFECT A
Cache 3
Cache 9
610
Bus 1
Bus 2
Bus 3
Bus 4
Bus 9
Bus 10
DEFECT
DEFECT B
µP2
µP3
µP9
310B
310
310
310

FIG. 7

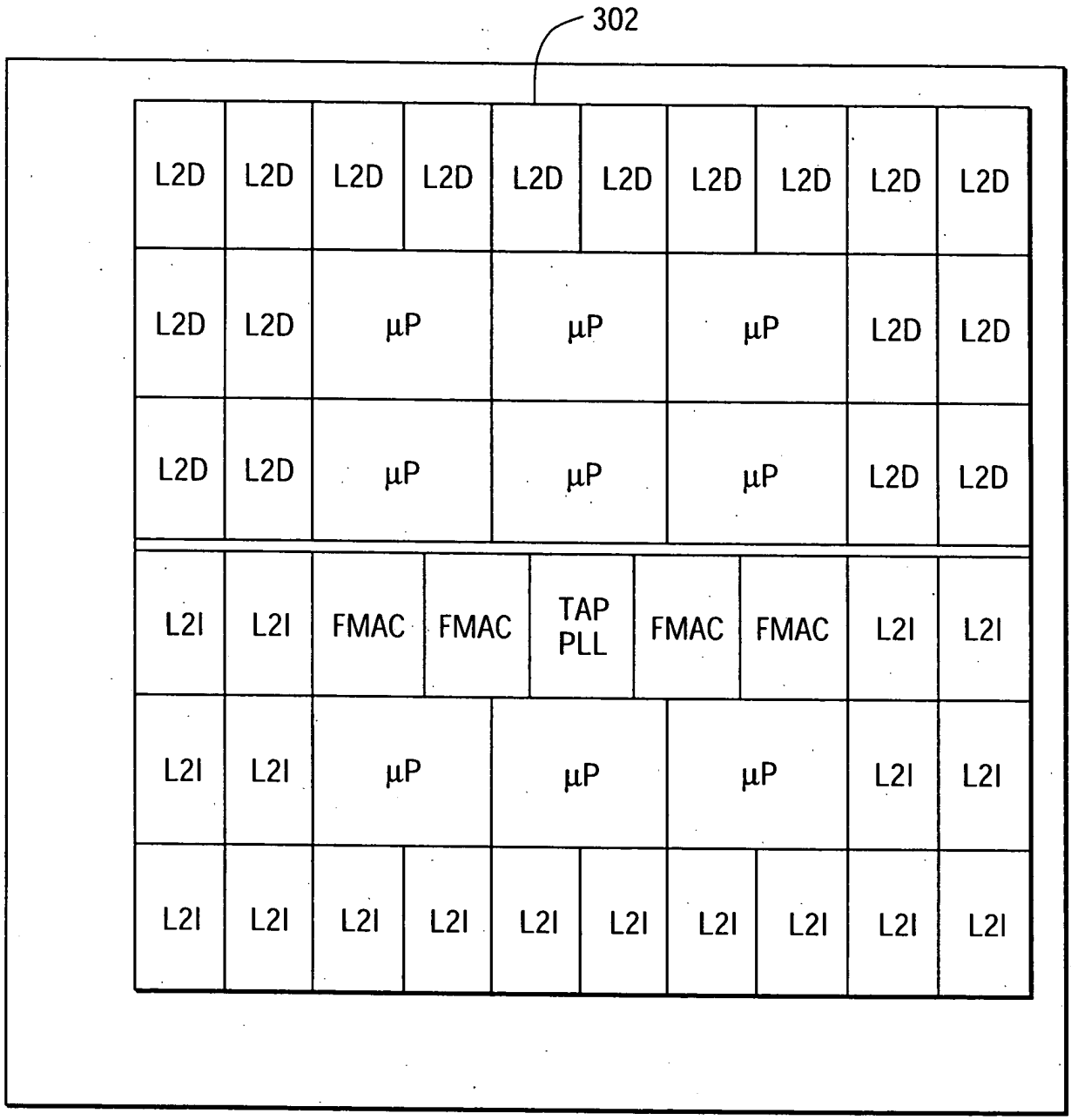
302
L2D
L2D
L2D
L2D
L2D
L2D
L2D
L2D
L2D
L2D
L2D
L2D
μP
μP
μP
L2D
L2D
L2D
L2D
μP
μP
μP
L2D
L2D
L2I
L2I
FMAC
FMAC
TAP PLL
FMAC
FMAC
L2I
L2I
L2I
L2I
μP
μP
μP
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I
L2I

FIG. 8

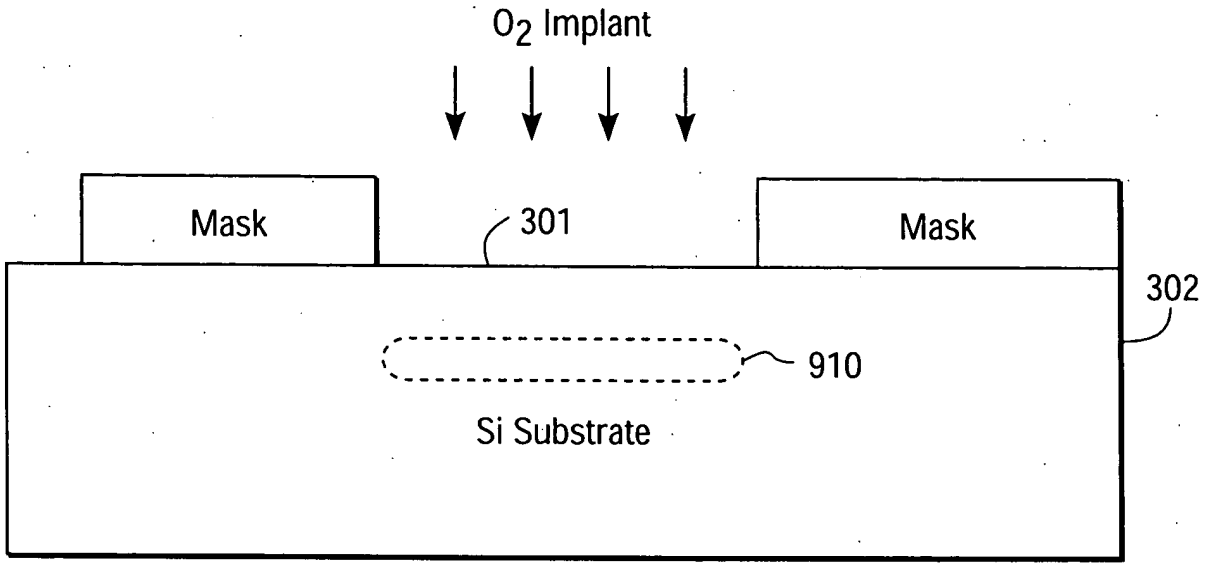
O_2 Implant
Mask
301
Mask
302
910
Si Substrate

FIG. 9

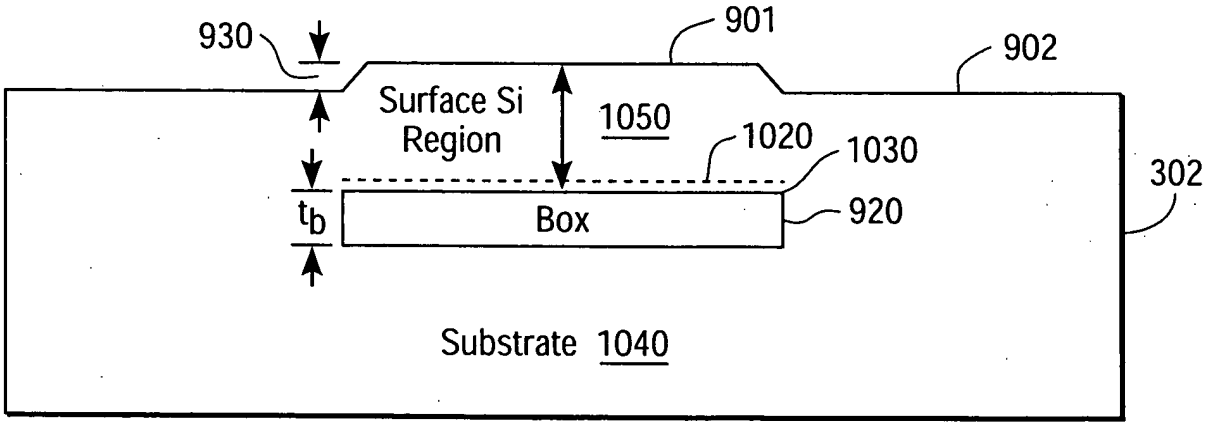
930
901
902
Surface Si Region
1050
1020
1030
t_b
Box
920
302
Substrate 1040

FIG. 10